



## PlanAhead – The Fastest Route to Better Design



### Today's complex FPGA designs involve a broad array of challenges:

- Unpredictable routing results and inconsistent performance levels
- PCB Integration issues due to FPGA pin-out problems
- Extensive and numerous design iterations
- Cost overruns, slipped schedules, and missed market opportunities

### PlanAhead™ allows you to:

- Reduce design iterations and maintain performance goals
- Establish FPGA I/O, even without a complete netlist
- Resolve routing congestion problems and timing issues
- Fit logic into smaller, less-expensive devices

PlanAhead provides an intuitive environment which delivers a faster, more efficient design solution to find and fix problems early, helping you achieve your performance goals.

#### Unmatched Performance

In a recent series of benchmark designs targeting the Virtex™-5 family of 65nm FPGAs, PlanAhead demonstrated an average of 15% faster performance than competing solutions. This performance edge can reduce project costs with a two speed-grade advantage.

#### Block-Based, Incremental Design

PlanAhead provides hierarchical, block-based, modular and incremental design methodologies, enabling designers to change only part of the design, leaving placement of the rest intact and shortening design iterations. PlanAhead helps you consistently maintain the required performance, even while making frequent changes.

#### Powerful Ease-of-Use

PlanAhead delivers an intuitive environment providing schematic, floorplan, or device views of your design. You can define and refine the hierarchy of your design for better results, or for more efficient use of resources to achieve optimal performance and greater utilization.

## ExploreAhead

ExploreAhead, integrated within PlanAhead, is an implementation exploration tool. By managing multiple implementation runs, ExploreAhead allows users to create, save, and share recipes or "strategies" of place & route options. ExploreAhead also allows users to execute multiple implementation runs based on strategies they've defined, or predefined strategies shipped as factory defaults.

## PinAhead Technology

PinAhead offers FPGA designers an intuitive solution to the complexities of managing the interface between their target FPGA and the PCB. Using PinAhead, FPGA designers can assign interface I/O groups to I/O pins simply by dragging them into a graphical representation of their FPGA. PinAhead provides DRC and WASSO compliant I/O assignment, simplifying the cumbersome process of I/O management. By considering the data flow from PCB to FPGA die, optimal pinout configurations can be achieved quickly, thus reducing internal and external trace lengths and routing congestion.

## Signal Integrity

PlanAhead provides functionality to check limits for Weighted Average SSO (WASSO) analysis, allowing designers to more easily manage ground bounce on I/O banks for better signal integrity. PlanAhead provides the capabilities needed to limit the amount of ground bounce present immediately at the output of the FPGA, and to prevent corruption of the operation of other devices driven by the FPGA.

Device Family Support		System Requirements
Virtex-5 SXT	Spartan-3AN	Microsoft Windows 2000 and XP Professional Sun Solaris 2.8/5.8, 2.9/5.9 Red Hat Enterprise Linux 3 (32 or 64 bit)
Virtex-5 LXT	Spartan-3A	
Virtex-5 LX	Spartan-3E	
Virtex-4 FX	Spartan-3	
Virtex-4 LX		
Virtex-4 SX		
Virtex-II Pro		
Virtex-II		

For details on device support as well as a list of features, visit [www.xilinx.com/planahead](http://www.xilinx.com/planahead)

## Take the Next Step

Visit [www.xilinx.com/planahead](http://www.xilinx.com/planahead) to download a free, 30-day PlanAhead evaluation. This free evaluation will let you explore the PlanAhead advantage for yourself. Get started with a step-by-step tutorial or see how you can improve your own design.

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