

## MYCAD EDUCATIONAL PACKAGES

For the students or the beginners trying to expose themselves and to learn the new design methodology using CAD tools, the low cost package, MyCAD Educational Packages Series, are useful. Even though the educational software has a limited database handling and capability, it is an excellent self-paced learning material with details of MyCAD usage and design examples to help you increase your design capabilities.

- Self learning of electronic and IC design with EDA tools
- Excellent for universities and training institute
- Easy to learn step by step with the tutorial book
- From electronic system/engineering design to IC design
- Reduced design size of MyCAD Expert Version

### **MyChip Station™ V6.4 Educational Packages:**

It consists of a Layout Editor and a Layout Verifier such as DRC, ERC, and LVS. It also contains a schematic editor and netlist extractor for circuit designing.

#### **MyChip Educational Software**

- LayEd(Layout Editor) : handles up to 10,000 objects
- MyDRC(Design Rule Checker): handles up to 10,000 objects
- LayNet(Netlist Extraction and Electrical Rule Checker): handles up to 10,000 objects
- MyLVS(Layout Ver. Schematic): LVS up to 500 devices
- CifGds(Database Converter): Stream in only
- SchEd(Schematic Editor): No limitation
- Logic2SPICE(SPICE Netlist Extractor): Extracts up to 500 devices

**MyChip Educational Book** : The contents of a book are as follows. 209 pages book, "CMOS VLSI Layout Artwork Design Design & Lab".

Chapter 1. Introduction

Chapter 2. CMOS Fabrication Process

Chapter 3. Logic Schematic Fundamentals

Chapter 4. VLSI Design Styles

Chapter 5. CMOS Layout Styles

Chapter 6. Routing Techniques

Chapter 7. Layout Considerations and Strategy for Design Changes

Chapter 8. Full Chip Layout and Issues

Chapter 9. Data Management and CAD Tools

### **MyVHDL Station™ V5.1 Educational Package:**

It consists of a VHDL simulator, VHDL synthesizer, and a Schematic Viewer. You can learn VHDL modeling & debugging, how to synthesis your VHDL netlist.

#### **MyVHDL Educational Software**

- MyVHDL(VHDL Simulator) :Compile source files up to 2,000 signals
- MySyn(VHDL Synthesizer): No limitation
- SchGen(Schematic Generator): No limitation
- SchEd(Schematic Editor): No limitation

**MyVHDL Educational Book** : The contents of a book are as follows. 349 pages book, "Design Practice with MyVHDL Station".

Chapter 1. Design Method of Digital Systems  
Chapter 2. PLD (Programmable Logic Device)  
Chapter 3. Basic VHDL Grammar  
Chapter 4. How to User Design Tools  
Chapter 5. Combinational Circuit Design  
Chapter 6. Sequential Circuit Design

### **MyLogic Station™ V5.1 Educational Packages:**

It consists of a Schematic Editor, a Logic Simulator, Waveform Analyzer and a Schematic Generator. You can learn the schematic design method, logic simulation, and schematic generation form EDIF data. The schematic data can be extracted to RT level VHDL netlist or EDIF netlist.

#### **MyLogic Educational Software**

- SchEd(Schematic Editor) : No limitation
- SchGen(Schematic Generator): No limitation
- MySim(Logic Simulator & Waveform Analyzer): Simulate up to 10,000 gates
- Logic2EDIF(EDIF 200 netlist generator): Handles up to 10,000 gates

**MyLogic Educational Book** : The contents of a book are as follows. 186 pages book, "Design Practice with MyLogic Station".

Chapter 1. How to Use the Schematic Editor(Part I)  
Chapter 2. How to Use the Schematic Editor(Part II)  
Chapter 3. How to Use the Logic Simulator  
Chapter 4. Configuration for Clock Circuit Design  
Chapter 5. 6-Digit Counter Design  
Chapter 6. Decimal Counter Design  
Chapter 7. 10-Digit Counter Design  
Chapter 8. Frequency Divider Design  
Chapter 9. MODESEL Block Design  
Chapter 10. Count Block Design of Hour, Minute, and Second  
Chapter 11. STOPWATCH  
Chapter 12. Block Design of SEL1 and SEL2  
Chapter 13. 7-Segment Decoder Block Design  
Chapter 14. Decoding Block Design  
Chapter 15. OUT Block Design  
Chapter 16. Overall Clock Circuit Design for Simulation  
Chapter 17. Overall Clock Circuit Design for FPGA  
Chapter 18. Making Clock Application Circuit Board for FPGA  
Chapter 19. Embodiment of Electronic Clock Circuit Using FPGA